A 25-102GHz 2.81-5.64mW Tunable Divide-by-4 in 28nm CMOS

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***Abstract*—A wideband tunable divide-by-4 is designed and realized in 28nm bulk CMOS. A systematic design methodology to maximize the locking range over power consumption ratio is proposed. The test chip core area is only 25.6x24.8µm^2 and measurements repeated over several samples demonstrate an operating frequency range from 25GHz to 102GHz with a maximum power consumption of 5.64mW from a 0.9V supply. The frequency band from 44.3GHz to 90GHz is covered in only three steps with a minimum fractional bandwidth in exceed of 20% and power consumption less than 4.7mW demonstrating the effectiveness of the proposed design techniques.**

Keywords—frequency divider, mm-Wave, CML dynamic latch, inductorless, low power, wideband, E-band, CMOS.

I. INTRODUCTION

Being the technology of choice for mass-production digital circuits, since the seventies CMOS has drawn an ever increasing attention from academia and companies. Transistors implemented in deep scaled technology nodes such as 28nm show a f_t of 300GHz, allowing the design of low power analog circuits at mm-Wave [1]. In this context, extensive research has been done recently to improve performance of PLL at these frequencies, being key building blocks of any transceiver for wireless applications. In state-of-the-art fundamental mm-Wave PLL (both analog and digital) the first divider and oscillator run at the highest frequency, becoming the system bottleneck for noise, tuning-range, power consumption and yield under PVT variation [2, 3]. It is therefore highly desirable to adopt robust low power solutions for the frequency divider, with possibly a large tuning capability to overcome the variation. Static CML dividers are famous for the wide locking range (LR), but require a large power consumption to work at high speed, even if inductive peaking techniques are used [4]. Injection locked LC frequency dividers on the other hand, achieve the higher speed for a given power consumption but need one or even more on-chip inductors rising the complexity of the design and yielding a large area consumption for a limited LR [5-9]. In [10] an RC static divider based on CML dynamic latches with load modulation is proposed. This topology, derived by the traditional CML static one, improves the divider performance at high frequencies, leading to a low power tunable solution. In this paper a systematic design methodology is presented to maximize performance of this last class of dividers in the frequency band from 60 to 90GHz (so called E-band). Several samples of the 25.6x24.8µm^2 prototype realized 28nm bulk CMOS are fully characterized, demonstrating a measured operating range from 25GHz to 102GHz, when drawing 2.81mW to 5.64mW from a 0.9V supply. Fig. 1 compares the tuning capabilities and power consumption of state-of-the-art divide-by-4, proving the effectiveness of the proposed design techniques.

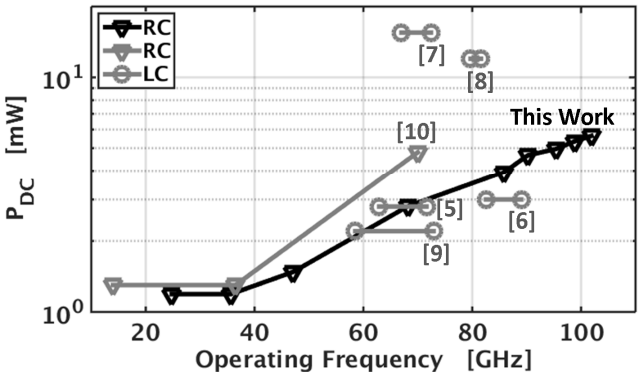

Fig.1. Comparison of mm-Wave CMOS divide-by-4. RC based dividers clearly show a superior tuning capability that makes them roboust against PVT variation. Moreover, getting rid of the on-chip inductor, they enjoy the full advantage of CMOS scaling (i.e. lower power, lower area and highier speed for each technology node).

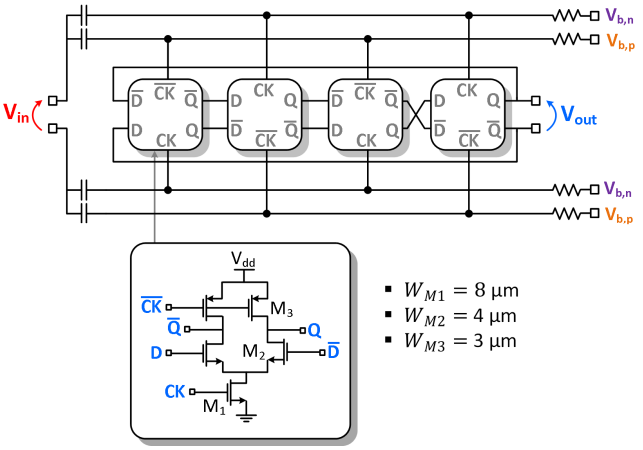

Fig.2. Divide-by-4 block diagram with AC coupling and DC bias (top). CML dynamic latch with load modulation schematic and transistors width (bottom). All transistor are minimal length.

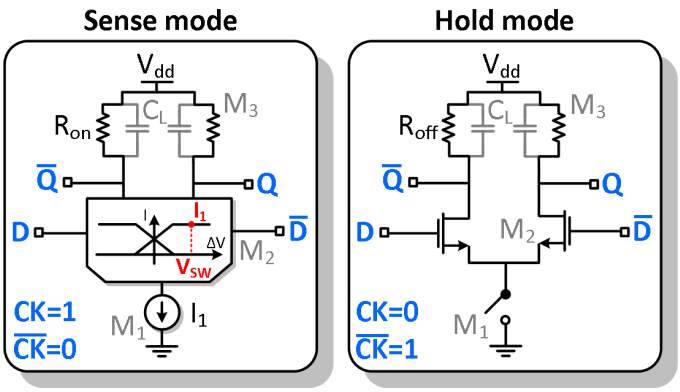

Fig.3. AC large signal model of the CML dynamic latch with load modulation during the sense mode (left) and during the hold mode (right).

II. TUNABLE DIVIDE-BY-4 BASED ON CML DYNAMIC LATCHES DESIGN

Fig. 2 shows the proposed divider based on the topology presented by Ghilioni et al., where four CML dynamic latches with load modulation are closed in a feedback loop, improving the maximum operation frequency (f_{max}) and locking range of the conventional divider based on static CML latches for a given power consumption [10]. The large signal operation principle of the divider is reviewed in II-A. A detailed systematic analysis based on post-layout simulation is presented in II-B, yielding design guidelines for optimal performance in the E-Band (i.e. 60 to 90GHz).

A. Lage Signal Circuit Operation Principle

The latch depicted in Fig. 2 consists of a differential pair where a complementary clock drives both the tail current source (M_1) and the PMOS load (M_3) biased in the triode region. The operation of the circuit can be divided in two regions: (1) sense mode when CK=1 and (2) hold mode when CK=0. The AC large signal model of the circuit during the two different states is shown in Fig. 3. During the sense mode, the differential pair charges the load parasitic capacitor C_L. The differential output voltage tends asymptotically to $R_{on}I_1$ with a time constant $R_{on}C_L$. A low value of $R_{on}C_L$ together with a large bias current is therefore beneficial to increase the speed of the latch during this phase. When the output differential voltage reaches V_{SW} (see Fig. 3), the differential pair of the following stage can be switched completely, ensuring the correct operation of the divider. This threshold sets the limit for f_{max}.

During the hold phase, on the other hand, the tail current source is switched off and the parasitic capacitance at the output is discharged through R_{off}. To ensure the correct operation in this phase, the differential output voltage should not drop below V_{SW}. Hence, a large value of $R_{off}C_L$ is desirable to extend the hold phase, setting a lower bound for f_{min}. Clearly, for given power consumption (imposed by I_1), W_3 sets the ratio R_{off}/R_{on} yielding a trade-off between LR and maximum operation frequency. By the same token, increasing

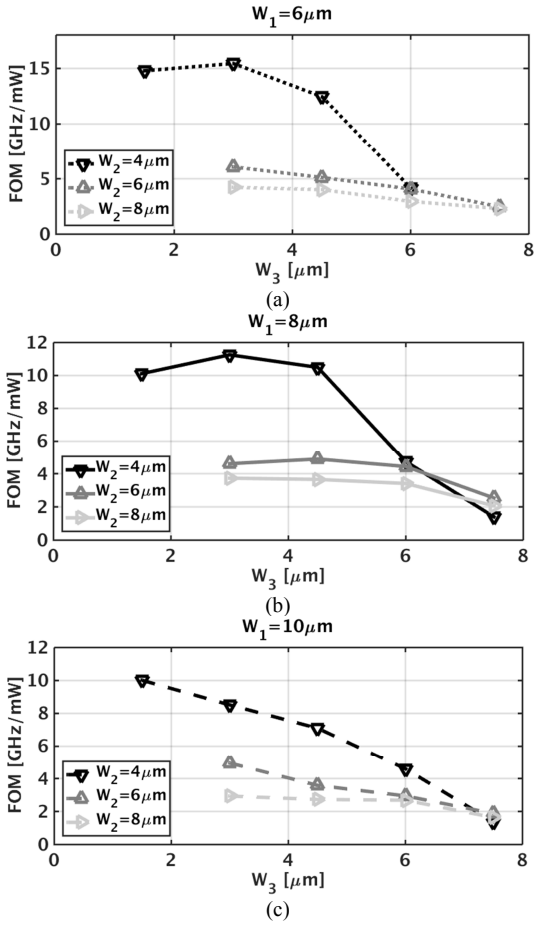

Fig.4. Simulated FOM versus the loading transistor width (W_3) for different sizes of the differential pair (W_2) when the width of the tail transistor is W_1=6μm (a), W_1=8μm (b), W_1=10μm (c). All transistor are minimal length. For fair comparison, the f_{SO} is set at about 80GHz for each configuration.

W_2 lowers V_{SW} at the cost of higher parasitic loading capacitance.

Assuming that the transconductors operate in the square-law region it is possible to write simple approximated close form equations for f_{max} and f_{min} [10]. Although this analysis is fundamental to get insight into the operation of the divider, it is important to remember that the Shichman-Hodges model holds true only for a narrow operation region in deep scaled CMOS and below 20nm this model has completely disappeared [1]. Moreover, not much has been reported so far about how the size and the bias point of M_1 affect the overall performance.

B. Design for Maximum Locking Range and Minimum Power Consumption in the E-Band

To achieve optimal performance in the frequency band from 60 to 90GHz, in this work a systematic design procedure is proposed. From the qualitative analysis given in II-A, it is clear that a high frequency of operation comes at the cost of a narrow locking range for the same power consumption. The optimal design is therefore the one that maximize the following Figure Of Merit:

$$FOM = LR / P_{DC} \quad (1)$$

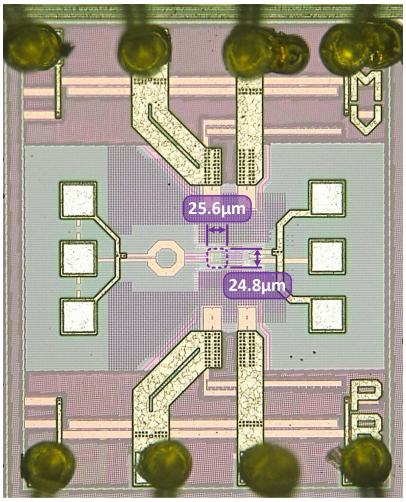

Fig.5. Die micrograph of the realized test chip (core dimensions: 25.6µm x 24.8µm).

If no RF transistor model is available during the design phase, to avoid misleading results it is mandatory to include from an early stage of the design the layout parasitics due to the low metal connections to the transistor. After a first investigation of the divider operation adopting digital transistor models at a schematic level, a first estimation of the device dimension is obtained. Then, different transistor layouts are drawn and a post layout parasitic extractor tool (e.g. PEX, QRC, etc…) is used to predict their effect on the device performance. All active devices are designed with minimal length for maximum speed (L=28nm). To characterize the quantitative behavior of the divider, the expected FOM is investigated for different device sizes. For each configuration the self oscillation frequency (f_{SO}) is set at about 80GHz by acting on bias current I_1 and the bias point of the loading transistor, through V_{bn} and V_{bp} respectively (see Fig. 2). In Fig. 4 the expected FOM is reported against the PMOS loading transistor width (W_3) for different sizes of the differential pair (W_2), when the divider is driven by a differential sinusoidal clock with amplitude 400mV 0-pk. The experiment is repeated for different sizes of the tail transistor, namely W_1=6µm (Fig. 4a), W_1=8µm (Fig. 4b), W_1=10µm (Fig. 4c). The LR/P_{DC} ratio improves when M_1 and M_2 are designed with a relatively small width. Moreover, in II-A an optimum value of R_{off}/R_{on} was expected. This sweet spot is evident in Fig. 4a-b for a value of W_3=3µm. The downside of reducing the width of M_1 and M_2 is that, for the same frequency of operation, the output voltage swing is reduced. When W_2=4µm and W_3=3µm the simulated differential voltage swing 0-pk is 715mV, 655mV and 530mV for W_1=10µm, W_1=8µm and W_1=6µm respectively. Further decreasing W_1 to 4µm leads to a 200mV 0-pk voltage swing and a drop of f_{max} in favor of a reduction in power consumption. This case is therefore not reported in Fig. 4. To account for possible device model inaccuracy, in this design the transistor are overdesigned to W_1=8µm, W_2=4µm and W_3=3µm to ensure wide margin of operation.

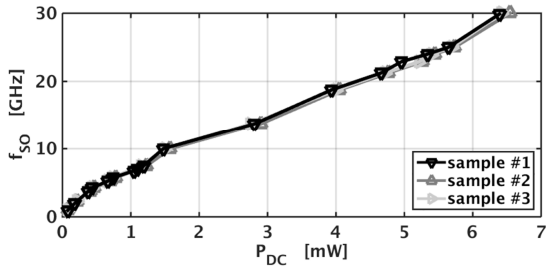

Fig.7. Measured divider self-oscillation frequency agaist power consumption from three samples. The maximum f_{SO} of 30GHz shows that the divider can operate up to f_{IN}=120GHz drawing less than 7mW from a 0.9V supply.

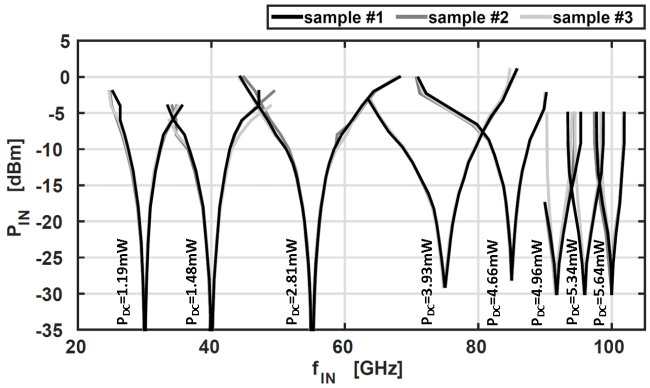

Fig.8. Measured divider sensitivity curve and power consumption from three samples.

III. Measurement Results

The die photograph of the divide-by-4 prototype realized in 28nm bulk CMOS technology is shown in Fig. 5. Since this topology does not rely on on-chip inductors, the resulting core area is only 25.6x24.8µm^2. The test chip and measurement setup block diagram is shown in Fig. 6. Measurements are performed on a high-frequency probe station. The DC pads are wire-bonded to a PCB while the input and output pads are accessed by 50Ω GSG probes. To demonstrate the wideband operation of the designed prototype at mm-Wave with the available measurement equipment, the spectrum is divided in three parts. An E8257D Agilent PSG is used to generate the input signal up to 67GHz. Two different source modules followed by a dedicated linear level set attenuator cover the band from 60 to 90GHz and from 90 to 140GHz respectively. For testing purpose, the input clock signal is applied to an on-chip transformer that serves as balun. A buffer is also implemented on-chip to drive the 50Ω measurement equipment. The output spectrum and phase noise is measured directly with a 43.5GHz R&S FSW Signal and Spectrum Analyzer.

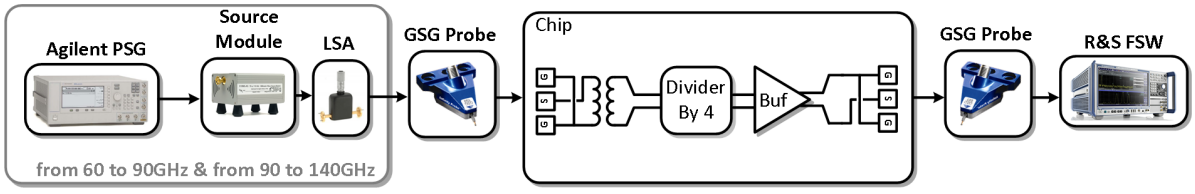

Fig.6. Divider test chip and measurement setup block diagram.

Several samples are fully characterized demonstrating a broad frequency of operation and negligible difference among each other. All the experiments are performed with a 0.9V supply. Fig. 7 shows the measured self oscillation frequency versus DC power consumption of the divider. By changing V_{bn} from 250mV to 700mV and V_{bp} from 660mV to 110mV, f_{SO} is tuned from 990MHz to 30GHz. Meaning that the divider can operate with an input frequency ranging from 4GHz up to 120GHz with a power consumption that increases almost linearly from 0.08mW to 6.5mW. Fig. 8 shows the measured sensitivity curves and respective power consumption. The prototype is locked from a 25GHz to a 102GHz input clock frequency, demonstrating a minimum and maximum locking range of 4.2% and 42.4% respectively. Noteworthy, the frequency band from 44.3GHz to 90GHz is covered in only three steps with a minimum fractional bandwidth in exceed of 20% and power consumption less than 4.7mW. Further characterization of the sensitivity curves under signal injection is limited by the band-pass behavior of the on-chip balun. In Fig. 9 the measured phase noise at the input and output of the divider for an 80GHz input clock frequency is reported. The expected $20\log_{10}(4)\approx12$dB phase noise reduction is demonstrate up to ≈5MHz. The phase noise far from the carrier is limited by the on-chip buffer. However, the noise contribution of the divider is low-pass filtered by the loop when employed in a PLL and the loop bandwidth of state-of-the-art mm-Wave PLLs is normally limited to 1.5-2MHz [2, 3].

Table I summarizes the performance and compares it with state-of-the-art mm-Wave divide-by-4 in bulk CMOS. This work shows the higher tuning capability and the lower area consumption. Moreover, Table 1 and Fig. 1 clearly show that, thanks to the presented design techniques, (1) the results reported in [10] are extended towards lower power and higher frequencies and (2) the use of on-chip inductors in (LC) dividers comes at the cost of large silicon area and poor tuning capabilities, while exacerbating the problem of magnetic coupling to and from other circuits, and with no obvious improvement with technology scaling.

IV. Conclusion

A systematic design methodology to maximize performance of wideband static dividers based on CML dynamic latches has been proposed. The presented 25.6x24.8μm^2 28nm CMOS divide-by-4 shows a measured operating frequency range from 25GHz to 102GHz for 5.64mW maximum power consumption. Measurements repeated on several samples show negligible differences. To the best of the authors' knowledge, this is the first time that a single low power divide-by-4 circuit is demonstrated with wide margin over the whole E-Band (60 to 90GHz) and beyond.

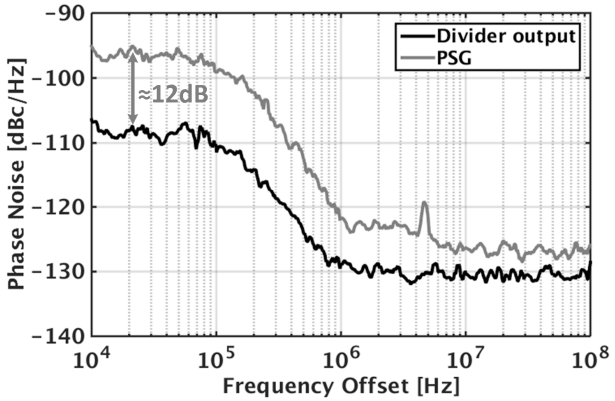

Fig.9. Input (grey) and output (black) measured phase noise from an 80GHz input frequency.

TABLE I. mm-Wave Divide-by-4 State-of-the-art

Ref.	f_{min}-f_{max} (GHz)	Locking Range (%)	P_{DC} (mW)	FOM[a] (GHz/mW)	Area (μm^2)	CMOS Tech. (nm)
[5]	62.9-71.6	3.2	2.8	0.82	14300	90
[6]	82.5-89	7.6	3	2.17	6380	90
[7]	67-72.4	7.7	15.5	0.35	661200	90
[8]	79.7-81.6	2.4	12	0.16	34980	65
[9]	58.5-72.9	21.9	2.2	6.55	41600	65
[10]	14-70	60-90[b]	1.3-4.8	6.67-17.5[b]	990	32
This work	**25-102**	**4.2-42.4[b]**	**2.81-5.64**	**0.74-8.49[b]**	**635**	**28**

[a] *FOM = Locking Range (GHz) / P_{DC} (mW)*

[b] *Worst - best*

Acknowledgment

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